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APPLICATION FOR LETTERS PATENT

FOR

BUBBLE HANDLING A/D CONVERTER CALIBRATION

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Bubble Handling A/D Converter Calibration

Cross Reference to Related Application

This application is a continuation of copending International Application No. PCT/SE02/00562 filed March 22, 2002, and claiming a priority date of March 26, 2001, which designates the United States.

Technical Field of the Invention

The present invention generally relates to handling of occurrences of bubbles on the thermometer code bus of a flash A/D converter or an A/D converter stage of a multi-stage A/D converter.

Flash A/D converters include a set of comparators that simultaneously convert an analog signal into thermometer code, which is converted into binary code. This conversion relies on detection of the location of the 1-to-0 transition in the thermometer code. However, due to component imperfections in the converter, there may in fact be several such transitions in the thermometer code. This is called a bubble or sparkle and leads to ambiguities in the conversion. References [1] S. Padoan, A. Boni, C. Morandi and R Venturi, "A novel coding scheme for the ROM of parallel ADCs, featuring reduced conversion noise in the case of single bubbles in the thermometer code", IEEE International Conference on Electronics, Circuits and Systems, 1998; [2] M. Sugawa, H. Yoshida, M. Mitsuishi, S. Nakamura, S. Nakaigawa, Y. Kunisaki and H. Suzuki, "A 2.5V 100MS/s 8bit ADC using Pre Linearization Input Buffer and Level Up DAC/Subtractor", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998; [3] Jy-Der David Tai, "Bubble evaporation circuit for eliminating bubble errors in thermal code and its method", US Patent No. 6 038 662 (as signed to Powerchip Semiconductor corp.); and [4] Andrew G. F. Dingwall, "Decoder error prevention apparatus for use in flash analog-to-digital converters", US Patent 5 023 613 (assigned to Harris Semiconductor Patents, Inc.);

describe different algorithms for handling bubbles in the thermometer code. The purpose of these algorithms is to avoid catastrophic conversion errors in the thermometer-to-binary decoder due to the existence of a bubble. However, although these methods are bubble tolerant, they still produce large errors and they do not attempt to eliminate generation of future bubbles.

Summary of the Invention

An object of the present invention is a calibration method and apparatus for a flash A/D converter or an A/D sub-converter in an A/D converter stage that reduce or eliminate occurrences of thermometer code bubbles.

This object can be achieved by a calibration method handling occurrences of thermometer code bubbles in an A/D sub-converter in an A/D converter stage, including the steps of:

- detecting two A/D sub-converter comparators causing a bubble;
- increasing the threshold of the bubble causing comparator having the lowest threshold by a first predetermined voltage; and
- decreasing the threshold of the bubble causing comparator having the highest threshold by a second predetermined voltage.

The first and second voltages can be fractions of the A/D sub-converter quantization step. The first voltage can be equal to the second voltage. The method may further include the steps of:

- determining the last A/D sub-converter comparator having a threshold that is smaller than an analog A/D sub-converter input signal;
- increasing the threshold of the determined comparator by a third predetermined voltage if a residual signal from the A/D converter stage falls below a

predetermined minimum level; and

- decreasing the threshold of the first A/D sub-converter comparator having a threshold that is larger than the analog A/D sub-converter input signal by a fourth predetermined voltage if the residual signal exceeds a predetermined maximum level.

The third and fourth voltages can be fractions of the A/D sub-converter quantization step. The third voltage can be equal to the fourth voltage. The thresholds can be modified by modifying comparator offsets.

The object can also be achieved by a calibration apparatus handling occurrences of thermometer code bubbles in an A/D sub-converter in an A/D converter stage, comprising: means for detecting two A/D sub-converter comparators causing a bubble; means for increasing the threshold of the bubble causing comparator having the lowest threshold by a first predetermined voltage; and means for decreasing the threshold of the bubble causing comparator having the highest threshold by a second predetermined voltage.

The apparatus may further comprise means for determining the last A/D sub-converter comparator having a threshold that is smaller than an analog A/D sub-converter input signal; means for increasing the threshold of the determined comparator by a third predetermined voltage if a residual signal from the A/D converter stage falls below a predetermined minimum level; and means for decreasing the threshold of the first A/D sub-converter comparator having a threshold that is larger than the analog A/D sub-converter input signal by a fourth predetermined voltage if the residual signal exceeds a predetermined maximum level. The apparatus may further comprise means for modifying the thresholds by modifying comparator offsets.

The object can also be achieved by a multi-stage A/D converter including a calibration apparatus handling occurrences of thermometer code bubbles

in an A/D sub-converter in at least one A/D converter stage, the calibration apparatus comprising means for detecting two A/D sub-converter comparators causing a bubble, means for increasing the threshold of the bubble causing comparator having the lowest threshold by a first predetermined voltage, and means for decreasing the threshold of the bubble causing comparator having the highest threshold by a second predetermined voltage.

The calibration apparatus may further comprise means for determining the last A/D sub-converter comparator having a threshold that is smaller than an analog A/D sub-converter input signal, means for increasing the threshold of the determined. comparator by a third predetermined voltage if a residual signal from the A/D converter stage falls below a predetermined minimum level, and means for decreasing the threshold of the first A/D sub-converter comparator having a threshold that is larger than the analog A/D sub-converter input signal by a fourth predetermined voltage if the residual signal exceeds a predetermined maximum level. The multi-stage A/D converter may further comprise means for modifying the thresholds by modifying comparator offsets.

The object can also be achieved by a flash A/D converter handling occurrences of thermometer code bubbles, comprising means for detecting two A/D converter comparators causing a bubble, means for increasing the threshold of the bubble causing comparator having the lowest threshold by a first predetermined voltage, and means for decreasing the threshold of the bubble causing comparator having the highest threshold by a second predetermined voltage.

The flash A/D converter may further comprise means for modifying the thresholds by modifying comparator offsets.

Briefly, the present invention identifies the A/D converter comparators that are responsible for a detected bubble and adjusts their thresholds to reduce or

eliminate the threshold crossover that caused the bubble. An advantage with this technique is that the A/D converter will eventually be bubble-free. This is an especially attractive feature for residual based correction methods in multi-stage A/D converters, such as pipeline, cyclic or sub-ranging A/D converters.

Brief Description of the Drawings

The invention, together with further objects and advantages thereof, may best be understood by making reference to the following description taken together with the accompanying drawings, in which:

Fig. 1 is a block diagram of a typical pipeline A/D converter;

Fig. 2 is a block diagram of a typical stage of the A/D converter in fig. 1;

Fig. 3 is a diagram illustrating signal behavior on the thermometer code bus during normal operation of the A/D converter stage in fig. 2;

Fig. 4 is a diagram illustrating the concept of a bubble on the thermometer code bus;

Fig. 5 is a flow chart illustrating a conceptual embodiment of the method in accordance with the present invention;

Fig. 6 is a flow chart illustrating another conceptual embodiment of the method in accordance with the present invention;

Fig. 7 is a block diagram illustrating an exemplary embodiment of an A/D converter calibration apparatus in accordance with the present invention;

Fig. 8 is a block diagram of an exemplary embodiment of an increase/decrease logic block (IDLB) in fig. 7;

Fig. 9 is a block diagram of an exemplary embodiment of a merge logic block (MLB) in fig. 7;

Fig. 10 is a block diagram of an exemplary embodiment of an up/down counter and calibrating D/A converter in fig. 7;

Fig. 11 is a block diagram of an exemplary embodiment of a combined

comparator and latch;

Fig. 12 is a block diagram of a simplified embodiment of an increase/decrease logic block (IDLB) in fig. 7; and

Fig. 13 is a block diagram of a simplified embodiment of a merge logic block (MLB) in fig. 7.

Detailed Description of the Preferred Embodiments

In the following description the same reference designations will be used for the same or similar elements.

The description below will describe the present invention with reference to a pipeline A/D converter. However, it is appreciated that the same principles may also be used for other multi-stage A/D converters, such as cyclic or sub-ranging A/D converters (although a cyclic converter only includes one stage, for the purposes of this application it is still considered as a multi-stage converter, since the stage is used several times). Furthermore, the bubble handling method described below is also applicable to single-stage flash A/D converters.

Fig. 1 is a block diagram of a typical pipeline A/D converter. An N-bit analog-to-digital conversion is performed in two or more stages, each stage extracting $\{N_1, N_2 \ldots N_K\}$ bits of information represented by the digital words $\{d_1, d_2 \ldots d_K\}$, where K is the number of pipeline stages. The first pipeline stage extracts the N_1 most significant bits using an N_1-bit *A/D* sub-converter 10. Then the estimated value is subtracted from the analog input signal *Vin* by using a D/A sub-converter 12 and an adder 14, leaving a residue containing the information necessary to extract less significant bits. Usually the residue is amplified by an amplifier 16 having a gain G_1 to establish the appropriate signal range for stage 2. These steps are repeated for all K stages, with the exception of the last pipeline stage, which does not need to produce an analog output and therefore has no D/A converter, adder or amplifier, but only an A/D

converter 10. The digital words $\{d_1, d_2 \ldots d_K\}$ are then combined to form the digital output word d_{out} in a unit 18 for time alignment and digital correction of A/D sub-converter data.

In order to simplify the following description, it is assumed that an A/D converter stage has a resolution of 3 bits. This number is sufficiently small to be manageable, but is also large enough to illustrate the essential features of a typical case. However, it is appreciated that in general the number of bits may be larger. This is especially the case for a single-stage flash A/D converter which typically may have a resolution of up to 10 bits.

Fig. 2 is a block diagram of a typical stage of the A/D converter in fig. 1. A/D sub-converter 10 includes a number of comparators COMP1-COMP7. One input terminal of each comparator is connected to a corresponding reference or threshold voltage T1-T7. These threshold voltages are formed by a threshold generator 20. The other input terminal of each comparator receives the analog input signal (the same signal to each comparator). The output signals from the comparators collectively form the digitized value in thermometer code. These signals are forwarded to D/A sub-converter 12 over a thermometer code bus, where they are transformed into a corresponding analog value. This value is subtracted from the original analog value in adder 14, and the residual signal is amplified by a gain equal to 4 in gain element 16.

Before the invention is described in detail, the concept of a thermometer code bubble will be explained with reference to fig. 3-4.

The thermometer coded signal is transformed into a binary coded signal in a thermometer/binary decoder 22. This process is illustrated in fig. 3. In this example a sample of the analog signal lies between thresholds T5 and T6. This implies that comparators COMP1-COMP5 will output "1", while comparators COMP6-COMP7 will output "0". Thus, the thermometer code will be 0011111, as illustrated in

the figure. Typically decoder 22 includes simple logic that finds the position of the 1-to-0 transition. This position is used to select a corresponding row in ROM containing binary codes.

The example described with reference to fig. 3 is accurate for an ideal A/D converter. However, imperfections in the A/D converter may result in slight shifts of the thresholds, as indicated by T2 in fig. 4. If these shifts are of the order of half the quantization step between two consecutive thresholds (which can be the case for high resolution converters), the order between two thresholds may be reversed, as indicated by T5 and T6 in fig. 4. If the sample happens to lie between these reversed thresholds, the result will be a "0" output trapped between two "1" outputs. This is called a "bubble". In the example this will generate the signal 0101111 on the thermometer code bus. It is appreciated that in this case there will be two 1-to-0 transitions, one between thermometer code lines 4 and 5, and a second transition between lines 6 and 7. Since the transition point determines the row to be looked up in ROM, there will now be an ambiguity as to which binary code is to be used.

In the prior art the described ambiguity has been partially resolved by various kinds of preprocessing of the thermometer code or by fault tolerant procedures. However, large A/D converter errors will still remain, since these approaches only avoid catastrophic errors. A better approach is to eliminate the reason for the occurrence of bubbles, which is the approach taken by the present invention.

Fig. 5 is a flow chart illustrating a conceptual embodiment of the method in accordance with the present invention. The procedure starts in step S1 by determining the thermometer code of the relevant bits of the next sample and by setting the code index i=1 (corresponds to first line on the thermometer code bus). The reason for bubbles, namely crossed decision levels, can be detected by the occurrences of 0- to-1 transitions in the thermometer code when going from lower to higher thermometer code positions (in fig. 4 such a transition occurs between positions (lines)

5 and 6). This is performed in step S2, which tests whether thermometer code *i* is less than thermometer code *i*+ 1. If this is the case, step S3 increases (steps up) threshold *i* by a first predetermined voltage and decreases (steps down) threshold *i*+ 1 by a second predetermined voltage. Preferably the predetermined voltages are equal and of the order of 5-25% of the quantization step. As an example, the correction voltage may be 1/16 of the quantization step. The procedure then proceeds to step S4, in which code index *i* is increased by 1. If the test in step S2 indicates that thermometer code *i* is not less than thermometer code *i* + 1, the procedure proceeds directly to step S4. Step S5 tests whether code index *i* is the last index (7 in fig. 4). If so, the procedure loops back to step S1. Otherwise the procedure loops back to step S2.

The described bubble handling method is useful in both single-stage flash A/D converters and in flash A/D converter stages of multi-stage or multi-step A/D converters, such as pipeline, sub-ranging and cyclic A/D converters.

The present invention is especially advantageous in multi-stage A/D converters using residual based correction methods, such as the method described in [5] Zigiang Gu and W, Martin Snelgrove, "A Novel Self-Calibrating Scheme For Video-Rate 2-Step Flash Analog-to-Digital Converter", IEEE Inter national Symposium on Circuits and Systems, Vol. 4, pp. 601-604, 1992; and [6] Zigiang Gu and W, Martin Snelgrove, "Application of a novel self calibration scheme to a video-rate pipelined multi-stage A/D converter", IEEE, 1992; since these methods heavily rely on a bubble-free thermometer code. Such an embodiment is illustrated by the flow chart in fig. 6. In this flow chart steps S1-S5 are the same as in the embodiment of fig. 5. If step S2 determines that there is no bubble at thermometer code position *i*, step S6 determines whether code *i* is greater than code *i*+1, i. e. whether this position corresponds to the thermometer code transition 1-to-0. If this is not the transition position, the procedure proceeds to step S4. Otherwise step S7 tests whether the residual signal from this converter stage exceeds a maximum allowable value. If so,

step S8 decreases threshold i+1 by a predetermined voltage. If the residual is not too large, step S9 tests whether it falls below a predetermined minimum allowable value. If so, step S10 increases threshold i by a predetermined voltage. Otherwise the procedure proceeds to step S4. Preferably the predetermined voltages in steps S8 and S10 are equal and of the order of 5-25% of the quantization step. These voltages may also be equal to the voltages in step S3. As an example, the correction voltage may be 1/16 of the quantization step. The maximum and minimum values may, for example, be the expected maximum and minimum residual values for an ideal A/D sub-converter.

Since the calibration method described with reference to fig. 6 relies on detection of an unambiguous 1-to-0 thermometer code transition, it is appreciated that it is sensitive to bubbles. Thus bubble elimination in accordance with the present invention is essential for proper operation of this method.

In the embodiment in fig. 6 the residual based calibration is inhibited when a bubble is detected. This is, however, not absolutely necessary. Although the calibration will be less accurate in the presence of bubbles, these bubbles will eventually be eliminated by the present invention, and thereafter the residual based calibration will not be influenced by bubbles.

In the methods described with reference to fig. 5 and 6 the thermometer code lines were examined in succession. However, as will be illustrated below with reference to 7-11, all lines may also be examined in parallel.

An exemplary embodiment of an A/D converter calibration apparatus will now be described with reference to fig. 7 -11.

Fig. 7 is a block diagram illustrating an exemplary differential embodiment of an A/D converter calibration apparatus in accordance with the present invention. The figure illustrates the calibration logic of the A/D sub-converter

comparator array of an A/D converter stage. Increase/decrease logic blocks (IDLB) 30 are positioned between each comparator pair in the array and also at the top and bottom of the array. These blocks determine whether the adjacent comparator transition levels should be increased, unchanged or decreased based on the comparator output codes and residual overflow and underflow signals *o* and *u*, respectively, from the succeeding A/D converter stage. The thermometer code inputs t_u and t_l, respectively, of the top and bottom IDLB-blocks have no connections to comparator outputs and are instead held at the (constant) potentials that would result from an extended comparator array within range input signals. Merge logic blocks (MLB) 32 associated with each comparator combine the increase/decrease signals from neighboring IDLB-blocks into a clock signal CLK and an UP/DOWN signal (the top outputs of the top IDLB-block and the bottom outputs of the bottom IDLB-block are not connected (NC) to any MLB-block). These signals control a respective up/down counter 34 that provides a respective calibrating D/A converter 36 with calibration data. The calibrating D/A converter is connected to the associated comparator, where it adjusts the comparator offset, thereby adjusting the comparator threshold.

Fig. 8 is a block diagram of an exemplary embodiment of increase/decrease logic block (IDLB) in fig. 7. Two AND gates A1 and A2 detect transitions and bubbles, respectively, from the thermometer codes of neighboring comparators. The transition signals T2BIN are propagated to thermometer/binary decoder 22 (fig. 3). In case of a detected bubble, transistor M pulls down line *b*. This signals a detected bubble to all IDBL-blocks, thereby inhibiting further activity (corresponding to steps S6-S10 in fig. 6) due to detected transitions. The static power consumption when line *b* is pulled down is of no concern, since the bubbles will be rapidly eliminated. When the bubble signal has been time aligned by a latch controlled by a clock phase signal Φ_s, the increase and decrease commands i_u. and d_l, respectively, can be given directly to the adjacent comparators. If there is no bubble, the transition signal passes AND gate A3, and after time alignment it is gated to both

signals u and o to determine if any decrement or increment signals d_u and i_l, respectively, should be passed on to the adjacent comparators.

Fig. 9 is a block diagram of an exemplary embodiment of a merge logic block (MLB) in fig. 7. The decrement or increment signals d_u and i_l, respectively, to a comparator are merged in OR gates Ol and O2. An OR gate O3 detects if there were any signals to the MLB-block, and an AND gate A6 gates the resulting signal with a clock phase signal Φ_h to avoid generation of false CLK pulses due to transients. The UP/DOWN signal is produced by O2 and is high only in the presence of increment signals. The CLK and UP/DOWN signals are used to control up/down counter 34.

Fig. 10 is a block diagram of an exemplary embodiment of an up/down counter and calibrating D/A converter in fig. 7. To avoid the counter to wrap around its lowest and highest values (0 and MAX) in case the calibration range is not adequate, the CLK signal is gated. The AND gates AL,x and AH,x in the counter chain are used to determine if the counter is at its minimum (0) *or* maximum (MAX) value, respectively. If it is at its minimum value, gates A7, A8, 04 and Nl will block clock pulses that would otherwise decrement the counter. On the other hand, if the counter is at its maximum value, further incrementing will be inhibited. The clock signal CLK to the positive edge triggered latches is inverted by NAND gate Nl to allow as much settling time as possible to the counter chain after a change in the UP/DOWN signal. By not using a continuous clock and only clocking the counters in the event of adjustments, which will be rare as soon as the calibration values have settled, unnecessary power consumption and circuit noise are avoided. A PRESET signal can be used to initially put the counter to its mid position by setting/resetting the latches, but this function is optional.

The up/down counter 34 controls switches S,x that direct the currents of current sources M,x to the CAL+ and CAL- branches of the output signal in accordance with the counter value. The directed currents are binary weighted to the

calibrating D/A converter output by a resistance network to form a differential voltage output corresponding to the counter value.

Fig. 11 is a block diagram of an exemplary embodiment of a combined comparator and latch. It is noted that the polarity of the calibration inputs are reversed with respect to the normal inputs for obtaining a correct adjustment of the threshold levels.

The embodiment described above with reference to fig. 7-11 performs both adjustments for removal of bubbles and for residual based calibration when the bubbles have been removed. However, in a flash A/D converter, which performs the digitalization of all bits in a single stage, no residual based calibration is possible (although other calibration methods may be used in this case). The same comment applies to the last stage in a multi-stage A/D converter. In these cases the IDLB-block and the MLB block may be significantly simplified, as illustrated in fig. 12 and 13, respectively.

The described embodiments adjust the thresholds by adjusting the comparator offsets. However, it is appreciated that the same principles may be used to adjust the thresholds directly in threshold generator 22 (fig. 2).

The present invention will allow an increase in performance, yield and/or simplified analog design, since the trade-off between speed and accuracy can be reduced. The offered possibility of continuous background calibration eliminates performance degradation due to drift while avoiding frequent disturbing interrupts for calibration.

It will be understood by those skilled in the art that various modifications and changes may be made to the present invention without departure from the scope thereof, which is defined by the appended claims.